ORDERING OF HIGH USE PROGRAM CODE SEGMENTS USING SIMULATED ANNEALING

Abstract of the Disclosure

An apparatus, program product and method utilize a heuristic-based algorithm such as simulated annealing to order program code segments in a computer memory to provide improved computer performance in terms of memory access, e.g., by minimizing cache misses or other memory-related performance penalties that may be present in a multi-level memory architecture. Program code is ordered in a computer memory by selecting an ordering from among a plurality of orderings for a plurality of program code segments using a heuristic algorithm, and ordering the plurality of program code segments in a memory of a computer using the selected ordering.

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